Automatic Analog IC Layout Generation based on a Evolutionary Computation Approach

Nuno Lourenço
Instituto de Telecomunicações
Av. Rovisco Pais, 1
1049-001 Lisbon, Portugal
nlourenc@gmail.com

Nuno Horta
Instituto de Telecomunicações
Av. Rovisco Pais, 1
1049-001 Lisbon, Portugal
n.horta@ieee.org

ABSTRACT
This paper describes an innovative analog IC layout generation approach based on evolutionary computation techniques.

Categories and Subject Descriptors
J.6 [**Computer-Aided Engineering**]: Computer-Aided Design.

General Terms
Algorithms, Design, Experimentation

Keywords
Analog ICs, Layout Generation, Evolutionary Computation

1. INTRODUCTION
As the evolution of global semiconductors market indicates a fast growth of integrated circuits with both analog and digital functionalities, the development of design automation tools has become a key factor to enhance the efficiency of integrated circuits design cycle. However, despite the development efforts, the use of design automation tools to support the analog integrated circuit design, in industrial environments, is still limited, when compared with the digital counterpart [1].

2. DESIGN APPROACH
The proposed automatic layout generation approach, described in fig. 1, starts by a template description which must be entered together with the target technology design kit.

The topological relations present in the template are extracted to a B-Tree layout representation, on which the O(n log n) packing algorithm presented in [2] is used to obtain a compact placement. To decide the optimal combination of modules an evolutionary optimization kernel is used.

The router uses the placement solution and the template's nets to produce the desired routing. The template based routing algorithm used is a two step procedure. The template routing is adjusted (re-scaled) to the newly created placement. Then, the optimizer attempts to improve the routing quality. The major challenge in the router is the design rules verifications; they make the routing algorithm more complex and computationally more expensive than the placement algorithm.

GECCO'07, July 7–11, 2007, London, England, United Kingdom
ACM 978-1-59593-697-4/07/0007.

The proposed design methodology was tested using a preliminary version of LAYGEN. Although the generation capabilities of the tool are not yet at the level required for practical uses, the prototype is running and the methodology was proven with selected examples, as illustrated in fig. 2.

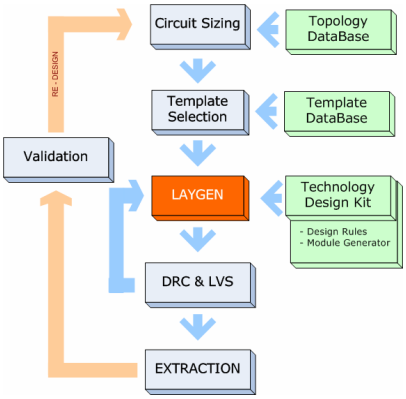

Figure 1. LAYGEN Automatic Layout Generation

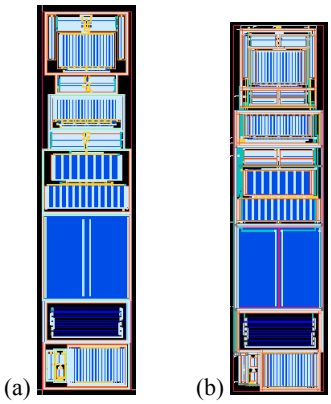

Figure 2: 2-Stage Cascade OTA (a) Automatic Layout Generation vs (b) Manual Design

3. REFERENCES
[1] G. Gielen and R. A. Rutenbar, "Computer-Aided Design of Analog and Mixed-Signal Integrated Circuits", in Proc. IEEE, vol. 88, pp. 1825-1852, Dec. 2000.

[2] F. Balasa, S.C. Maruvada, K. Krishnamoorthy, "Using Red-Black Interval Trees in Device-Level Analog Placement with Symmetry Constraints," in Proc. ASP-DAC 2003, pp. 777-782, Jan. 2003.