
EHWPack: a Parallel Software/Hardware Environment for Evolvable Hardware

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Abstract

This paper describes the EHWPack development system, a multi-tasking parallel software tool that performs the evolutionary synthesis of electronic circuits, using the SPICE simulator and the Field Programmable Transistor Array hardware (FPTA) developed at JPL (Stoica, 1999). EHWPack integrates free and commercial software packages such as PGAPack for the evolutionary algorithm, Spice 3F5 for the circuit evaluation, Tcl-Tk for the graphic interface, and LabView for the hardware evaluation. The paper investigates the performance of the tool in two typical problems of EHW: evolutionary synthesis of a Gaussian computational function and the evolution of a band-pass filter.

The EHWPack is a distributed parallel software-hardware environment for evolutionary synthesis and optimization of electronic circuits. It has also been used as a test-bed for new architectures of reconfigurable hardware and nano-electronic devices (Stoica, 1999). It runs on the HP Exemplar Caltech parallel supercomputer and is remotely controlled from a local workstation. An interface code links the GA with the circuit simulator and with the hardware where potential designs are evaluated, while a graphic user interface (GUI) allows easy problem formulation. EHWPack has been developed to facilitate experiments, both in simulated as well as hardware evolution, using SPICE circuit simulator and a reconfigurable VLSI chip, the Field Programmable Transistors Array (FPTA), respectively (Stoica, 2000). EHWPack allows also experimentalists located at different sites, to design, optimize and test circuits using evolutionary algorithms in a user friendly, transparent and expeditious manner.

The FPTA cell is an array of transistors interconnected by programmable switches. The status of the switches (ON or OFF) determines a circuit topology and consequently a specific response. Thus, the topology can be considered as a function of switch states, and can be represented by a binary sequence, such as "1011...", where by convention

one can assign '1' to a switch turned ON and '0' to a switch turned OFF. The current FPTA cell consists of 8 transistors and 24 programmable switches. To offer sufficient flexibility, the cell has all transistors terminals connected via switches to expansion terminals, which allows the implementation of bigger circuits by cascading FPTA cells.

Using the EHWPack, we were able to synthesize a Gaussian computational function and a band-pass filter tuned to the AM band (Zebulum, 2000) in less than 4 minutes, using 1, 2 or 4 FPTA cells. The experiments were performed in hardware and in simulation. In the latter, 128 processors of the parallel supercomputer have been used. The same job took 1 hour 30 minutes in simulation on 1 processor. The experiments confirm that, to obtain maximum efficiency, the number of processors should be equal to the number of individuals evaluated at each generation. Finally, we observe that the time to evaluate one individual in hardware (10 ms) is the same on the FPTA or on the SPICE simulator running on 128 processors, but was one order of magnitude faster than the SPICE simulator running on 1 processor.

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References

- Stoica, A, et al. (1999). Evolutionary experiments with a fine-grained reconfigurable architecture for analog and digital CMOS circuits. In, *Proc. of the First NASA/DoD workshop on Evolvable Hardware*. Los Alamitos, CA: IEEE Computer Society Press.
- Stoica, A et al. (2000) Mixtrinsic Evolution. In *Proc. of the third Int. Conf. on Evolvable Systems*, Edinburgh, UK, Springer-Verlag.
- Zebulum et al.. (2000) A Flexible Model of a Field Programmable Transistor Array Targeted For Hardware Evolution. In the *Proc. of the Third Int. Conf. on Evolvable Systems*, Edinburgh, UK.. Springer Verlag.